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EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,112	STOCKINGER ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 9, 14, 16,17, 22 - 31* is/are rejected.

7)☒ Claim(s) *10 - 13, 15, 18 - 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/10/03* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Objections

1. Claim 8, line 6 should be retyped as follows: "is [a] at a second voltage".

2. Claim 5, line 14, claim 9, line 11 should be retyped as follows: "a [the] second output".

3. Claim 28, line 4, should be retyped as follows: "[the] a third bus".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is that it states: "during an ESD event, the third bus is at higher voltage than the first bus". It is not clear from the claim language, what voltage of the first bus is implied, a normal voltage or a voltage under ESD stress. For purpose of examination it was assumed that the fist bus voltage is the voltage under normal conditions.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 26, 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller (US 5,301,084). Regarding Claim 26, Miller discloses the trigger circuit including a detection circuit for detecting an ESD event (elements 84 and 86 in Fig. 5); an internal node (between elements 84 and 86 in Fig.5), the detection circuit detecting an ESD event via the internal node; wherein during normal operation, the internal node is coupled to a first bus (bus 22 in Fig.5); wherein during an ESD event, the internal node is coupled to a second bus (bus 18 in Fig.5) via a pull-up circuit (element 84 in Fig.5).

Regarding Claim 27, Miller discloses the trigger circuit wherein during normal operation, the second bus is at a greater voltage than the first bus (voltage of the power supply bus 18 is higher than the voltage of the ground bus 22 in Fig. 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 5, 8, 14, 16, 22 – 25, 28 - 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US 5,301,084) in view of Takeda et al. (US 6,385,021) and Worley et al., Sub-Micron Chip ESD Protection Schemes which Avoid Avalanching Junctions. Regarding Claim 1, Miller discloses a first bus; a second bus; a third bus

(DVCC, VCC, VSS and DVSS in Fig. 8); a shunting circuit including a plurality of transistors (elements 122, 123, 112, 96 in Fig. 8), the shunting circuit having a plurality of control terminals (transistor bases), a first current terminal coupled to the first bus (emitter of 122 is coupled to DVCC in Fig. 8), and a second current terminal coupled to the second bus (emitter of 134 is coupled to DVSS in Fig. 8), wherein the shunting circuit is made conductive to provide a discharge path from the first bus to the second bus for current from an electrostatic discharge (ESD) event (conductive paths are shown in Fig. 9). It further discloses the trigger circuit (shown in Fig.5) associated with each of plurality of MOS transistors, such as transistor 32 in Fig. 5 and the pad coupled to the first bus, second bus and the third bus (element 14 in Fig. 8). However, it does not disclose a trigger circuit triggering a plurality of protecting transistors. Takeda et al. disclose a trigger circuit (element 37 in Fig. 3) having its outputs coupled to a first control terminal (buffer 42 in the leftmost I/O CIRCUIT 30 in Fig. 3) of the plurality of control terminals of the shunting circuit to provide a first control signal and to a second control terminal (the BUFFER in another I/O CIRCUIT in Fig. 3) of the plurality of control terminals of shunting circuit to provide a second control signal, the trigger circuit is coupled to the third bus (ESD BUS in Fig.3). Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Miller solution by adding the central trigger circuit triggering all the protection transistors, because as Taked et al. state (col. 2, line 66 – col.3, line 15), "such clamp circuit encompasses a large substrate area" and "the area

utilized by trigger circuit commonly represents up to 50% of the total clamp circuit area". Therefore using a single trigger circuit for plurality of protection transistors will save the substrate space. Additionally Miller does not disclose a plurality of transistors in a stacked configuration. Worley et al. disclose a plurality of transistors in a stacked configuration (elements P1 and P2 in Fig. 7). Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Miller solution by adding the plurality of the stacked transistors according to Worley et al., because as Worley et al. state (pages 1.2.6 – 1.2.7), this measure would allow use of clamps for higher voltages exceeding the maximum voltage of transistors. As to the first and the second outputs of the trigger circuit coupled to the control terminals of the plurality of transistors, Worley et al. disclose such outputs (from transient and threshold detectors in Fig.6 and 7), which are coupled to the control terminals of transistors (P1 and Pp2 in Fig. 7). As to motivation for modification of the primary reference, it is the same as above.

Regarding Claims 2 and 3, Miller discloses a pull-up device (element 138 in Fig. 8); the pad (element 14 in Fig. 8) is coupled to the third bus (DVCC in Fig. 8) via the pull-up device. The pull-up device is in a diode-like configuration (col.9, lines 36 – 43).

Regarding Claim 4, Worley et al. disclose the first output and the second output (outputs of the transient detector and threshold detector in Fig. 5) are pulled to substantially a voltage of the third bus (Vesd bus in Fig. 7) to make conductive the shunting circuit (transistors P1 and P2 in Fig. 7) to discharge current of the ESD event

from the first bus to the second bus (from the Vdd PAD to the Vss pad in Fig. 7). As to motivation for modification of the primary reference, it is the same as above.

Regarding Claim 5, Worley et al. disclose the trigger circuit having the first switch and the second switch (transistors P1 and P2 in Fig. 7), which being made conductive to allow the ESD discharge. However, it does not disclose providing a current path between the third bus and the first output and between the third bus and the second output. Taked et al. disclose providing a current path between the third bus (ESD BUS in Fig. 3) and the first output (the leftmost I/O element in Fig. 3) and between the third bus and the second output (the second from the left I/O element in Fig. 3). Both references have the same problem solving area, namely providing ESD protection for semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Miller solution by adding the second output connected the same way as the first output according to Takeda et al., because modern integrated circuit mostly have the plural outputs, which have similar protection against ESD.

Regarding Claim 8, Worley et al. disclose the integrated circuit wherein during a normal operation the first output (node 2 in Fig. 7) is at a first voltage, and the second output (node 3 in Fig. 7) is at second voltage, the first voltage is inherently different from the second voltage.

Regarding Claim 14, Miller discloses a slew rate detection circuit (shown in Fig. 5) for detecting an ESD event.

Regarding Claim 16, Worley et al. disclose the transistors of the plurality as MOSFETS. A motivation for modification of the primary reference, it is the same as above.

Regarding Claim 17, Takeda et al. disclose a second shunting circuit including a plurality of transistors (such as 76 and 78 in Fig. 4), the second shunting circuit having a first current terminal coupled to the first bus (ESD BUS in Fig. 4) and a second current terminal coupled to the second bus (Vss BUS in Fig. 4), wherein the second shunting circuit is made conductive to provide a discharge path from the first bus to the second bus for current from an ESD event.

Worley et al. disclose the first output of the trigger circuit being coupled to a first control terminal (at node 3 in Fig. 7) of the shunting circuit (transistor P1 in Fig. 7) to provide the first control signal and the second output (at node 2 in Fig. 7) coupled to the second control terminal of the second shunting circuit (transistor P2 in Fig. 7) to provide the second control signal. Worley et al. additionally disclose a plurality of transistors in a stacked configuration (elements P1 and P2 in Fig. 7). A motivation for modification of the primary reference is the same as above.

Regarding Claim 22, Miller discloses a second pad (I pad in Fig. 8) coupled to the first bus, the second bus, and the third bus (through unmarked transistor in Fig. 8).

Regarding Claim 23, Miller discloses the integrated circuit operates at a first supply voltage (VCC in Fig.8), while the pad (elements 12 and 14 in Fig.3, 8) is coupled to receive external signals at a second voltage (DVCC in Fig. 8), which is higher than the first voltage (col. 8, lines 18 – 25).

Regarding Claim 24, Miller discloses the trigger circuit implemented with a plurality of transistors (elements 32 and 66 in Fig. 5). Both transistors inherently have a maximum voltage. However, it does not disclose a boost bus having a voltage during normal operation higher than the maximum voltage of transistors. Maloney et al. disclose the trigger circuit (at the bottom of Fig.3) coupled to the bus (hi-Vcc in Fig.3) having up to three times nominal Vcc, which is above maximum voltage of transistors. Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Miller solution by adding the plurality of the stacked transistors according to Maloney et al., because as Maloney et al. state (High-Voltage PMOS Clamps), this measure would allow use of clamps for higher voltages.

Regarding Claim 25, Miller discloses the third bus (DVCC in Fig. 8), which normally has a voltage higher than the first bus (VCC in Fig.8). Therefore, under ESD conditions, the third bus voltage will be higher than the first bus voltage.

Regarding Claim 30, Worley et al. disclose providing, in response to detecting an ESD event, a first control signal and a second control signal (at nodes 3 and 2 in Fig. 7) at a voltage substantially equal to a voltage of a first bus of an integrated circuit (Vdd, page 1.2.7 col. 2) to a first control terminal and a second control terminal, respectively, of a shunting device (transistors P1 and P2 in Fig. 7), wherein the first control signal and the second control signal being at the voltage makes conductive the shunting circuit to discharge current of the ESD event from a second bus to a third bus (page 1.2.7.col. 1,

2); providing, during a normal operation of an integrated circuit, the first control signal at a second voltage (at node 3 in Fig. 7) and the second control signal at a third voltage (at node 2 in Fig. 7), wherein the second voltage is less than third voltage, since the third voltage is equal to Vdd (from Vdd PAD), while the second voltage is lower at least 0.7V (the voltage drop across D1).

Regarding Claim 31, Worley et al. disclose selection of the second voltage and the third voltage such as keep normally the shunting transistors off and to minimize leakage current through the shunting circuit (page 2A.2.6 and Fig. 10).

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Worley et al. Miller discloses all the elements of Claim 26. However, regarding Claim 28, they do not disclose the internal nodded of the trigger circuit being coupled to the third bus. Worley et al. disclose the pull-up circuit including a capacitive pull-up device (element P3 in Fig. 7), wherein the internal node (node 2 in Fig. 7) is coupled to the third bus (Vesd bus in Fig. 7) via the capacitive pull-up device. A motivation for modification of the primary reference is the same as above (see Claim 1 rejection).

Regarding Claim 29, Worley et al. disclose a first output (node 3 in Fig. 7) and a second output (node 2 in Fig.7); during an ESD event, the trigger circuit providing at the first output and the second output, a first voltage (voltage of Vss bus in Fig. 7); wherein during normal operation, the trigger circuit providing a second voltage (voltage of Vesd

bus) at the first output and a third voltage (voltage of Vdd PAD in Fig. 7) at the second output, the second voltage being different than the first voltage.

Claims 6, 7 and 9 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US 5,301,084) in view of Takeda et al. (US 6,385,021), Worley et al., and Murakami (5,034,845). Miller, Takeda et al. and Worley et al. disclose all the elements of Claim 1. However, regarding Claim 6, they do not disclose a first and second outputs being pulled to different voltages. . Murakami disclose the ESD protection circuit having a plurality of outputs (OUT1, OUT2 in Fig. 4). During a normal operation the first and second outputs are inherently pulled to different buses having different voltages, such as the first output can be pulled to the fourth bus (VCCb in Fig. 4), while the second output is pulled to the second bus (GNDb in Fig. 4) since the outputs are controlled by different internal circuits (shown at the bottom of Fig. 4) and therefore a combination, when the first output carries logic 1, while the second output carries logic 0 is a quite routine state of the circuit. Both references have the same problem solving area, namely ESD protection of the semiconductor circuits having plural power supplies. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Miller solution by introducing additional output according to Murakami, because modern integrated circuits very often have a plurality of independent outputs.

Regarding Claim 7, in the Miller circuit modified according to Murakami, when the transistors pull the first and the second outputs to different buses, and therefore to

different voltages, the voltage drop across each of the transistors must be lower than the maximum of the transistor. This rule is ABC of the design. Violation of the basic design rules by designer would result in manufacturing substandard equipment.

Allowable Subject Matter

1. Claims 10 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that the claim recites the trigger circuit having an internal node, which under normal conditions is pulsed to a voltage of a fourth bus. Such limitation was not found in the collected prior art of the record. Claim 15 is objected to due to similar reason, since it recites a fourth bus.

2. Claims 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that the claim recites a fourth and the fifth busses, while the first control terminal is coupled to the first output via the fourth bus and the second control terminal is coupled to the second output via the fifth bus. Such limitation was not found in the collected prior art of the record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571)

272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
02/28/2005

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